DECLARATION

I, Young-Woo PARK, Korean Patent Attorney of 5F., Seil Building, 727-13, Yeoksam-dong, Gangnam-gu, Seoul, Korea do hereby solemnly and sincerely declare as follows:

1. That I am well acquainted with the English and Korean languages.
2. That the following is a correct translation into English of the accompanying certified copy of Korean Patent Application No. 2003-11794.

and I make the solemn declaration conscientiously believing the same to be true.

Seoul, May 2, 2006

Young Woo Park

Young-Woo PARK

THE KOREAN INDUSTRIAL PROPERTY OFFICE

This is to certify that annexed hereto is a true copy from the records of the Korean Industrial Property Office of the following application as filed.

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Applicant : Samsung Electronics Co., Ltd.

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COMMISSIONER

PATENT APPLICATION

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Title of the Invention : METHOD OF FORMING CAPACITOR OF SEMICONDUCTOR DEVICE

Dated this: March 18, 2003
To the COMMISSIONER

[ABSTRACT OF DISCLOSURE]

[ABSTRACT]

Disclosed is a method of forming a capacitor having a reaction-preventing layer of a semiconductor device. First, a first conductive layer is formed on a substrate as a lower electrode. Then, a reaction-preventing layer is formed on the first conductive layer to prevent an oxidation at a temperature of not generating a phase change of the first conductive layer. Thereafter, a dielectric layer is formed on the reaction-preventing layer and a second conductive layer is formed on the dielectric layer. The process for forming the capacitor is implemented at a low temperature. The generation of a defect due to a thermal damage can be remarkably decreased.

[REPRESENTATIVE FIGURE]

FIG. 1d

[SPECIFICATION]

[TITLE OF THE INVENTION]

METHOD OF FORMING CAPACITOR OF SEMICONDUCTOR DEVICE

[BRIEF DESCRIPTION OF THE DRAWINGS]

The above object and advantages of the present invention will become readily apparent by reference to the following detailed description when considered in conjunction with the accompanying drawings wherein:

FIGS. 1a to 1d are cross-sectional views for explaining a method of forming a capacitor of a semiconductor device according to a preferred embodiment of the present invention;

FIGS. 2a to 2g are cross-sectional views of explaining a method of forming a cylindrical capacitor of a semiconductor device according to a preferred embodiment of the present invention; and

FIG. 3 is a graph illustrated for explaining a contact resistance of a capacitor formed according to a preferred embodiment of the present invention.

[DETAILED DESCRIPTION OF THE INVENTION]

[PROPOSE OF THE INVENTION]

[THE AREA TO WHICH THE INVENTION PERTAINS AND THE PRIOR ART]

The present invention relates to a method of forming a capacitor of a semiconductor device, and more particularly, to a method of forming a capacitor

for preventing an oxidation of a lower electrode of a capacitor in a semiconductor device.

Generally, a DRAM device in a semiconductor device includes one access transistor and one storage capacitor.

The size of the capacitor should be decreased to satisfy a memory device having an increased integration degree. Accordingly, a method of forming a capacitor having a decreased size and a high storage capacitor becomes a subject of importance. Practically, a development on a method of increasing the storage capacity of the capacitor while maintaining a horizontal area of the capacitor occupied on a substrate becomes a new issue.

As widely known, the storage capacity of the capacitor C is represented by an equation as follows.

[Equation 1]

$C = \varepsilon 0 \varepsilon \times A / d$

In the above Equation 1, parameter $\varepsilon 0$ and ε, respectively, represents a dielectric constant in vacuum and a dielectric constant of a dielectric layer of a capacitor, A represents an effective area of the capacitor and d represents a thickness of the dielectric layer.

Referring to Equation 1, various methods for increasing the storage capacity of the capacitor can be considered such as a method of forming a dielectric layer having a high dielectric constant, a method of increasing an effective area of the capacitor, a method of reducing a thickness of the dielectric layer, a method of forming a dielectric layer using a ferroelectric material, etc. can be considered.

Accordingly, metal oxides having a high dielectric constant including Ta2O5, TiO2, Al2O3, Y2O3, ZrO2, HfO2, BaTiO3, SrTiO3, etc. are recently used for forming the dielectric layer.

An example of a capacitor having a dielectric layer including such metal oxide having a high dielectric constant is illustrated in U.S. Pat. No. 5,316,982 issued to Taniguchi.

The formation of the dielectric layer using metal oxide having a high dielectric constant is accomplished under an oxygen atmosphere. Therefore, during forming the dielectric layer, an oxide layer is sometimes formed at an interface between the dielectric layer and a lower electrode due to the oxygen atmosphere. When the oxide layer is formed at the interface between the dielectric layer and the lower electrode, the storage capacity of the capacitor is lowered.

Considering this problem, a nitride layer is formed on the lower electrode before forming the dielectric layer to prevent the formation of the oxide layer between the dielectric layer and the lower electrode and to prevent a reaction that may possibly occur between the dielectric layer and the lower electrode.

Here, the nitride layer is usually formed by a rapid thermal nitration (RTN) method. For example, a polysilicon layer is formed as the lower electrode and the surface portion of the polysilicon layer is nitrated by the rapid thermal nitration method to form the nitride layer. Generally, the rapid thermal nitration method is carried out at a temperature of about 700°C or over.

However, because the rapid thermal nitration is implemented at a

temperature of about 700°C or over, a thermal budget is applied to the lower electrode or a contact portion of a metal wiring. The thermal budget applied onto the lower electrode or the contact portion becomes a factor of lowering the function of a capacitor and therefore, of lowering the function of a semiconductor device.

Therefore, a method of forming the nitride layer on the lower electrode at a low temperature is recently applied instead of the rapid thermal nitration method.

Examples of forming the nitride layer on the lower electrode at the low temperature are disclosed in Korean Laid-Open Patent Publication Nos. 2002-32285 and 1999-55201.

According to the disclosures, a method of forming the nitride layer on the lower electrode by using a plasma nitration method and then forming Ta_2O_5 dielectric layer is disclosed. Here, when Ta_2O_5 layer is formed as the dielectric layer, a heat treatment should be implemented after forming the Ta_2O_5 layer. That is, the Ta_2O_5 layer is crystallized and impurities are removed through the heat treatment. However, the heat treatment is implemented at a temperature of about 700°C or over. Therefore, the lower electrode receives a thermal damage through the heat treatment to deteriorate the function of the capacitor.

As described above, when the capacitor is formed by the conventional method, various problems due to the formation of the oxide layer or a thermal damage may be generated.

[TECHNICAL OBJECT OF THE INVENTION]

Accordingly, the present invention has been made to solve the aforementioned problems, and a feature of the present invention is to provide a method of forming a capacitor at a low temperature even though the capacitor includes a metal oxide layer having a high dielectric constant as a dielectric layer.

[CONTRUCTION AND OPERATION OF THE INVENTION]

In accordance with one aspect of the present invention, there is provided a first method of forming a capacitor. First, a first conductive layer is formed on a substrate. Then, a reaction-preventing layer is formed on the first conductive layer to prevent an oxidation at a temperature of not generating a phase change of the first conductive layer. A dielectric layer is formed on the reaction-preventing layer and a second conductive layer is formed on the dielectric layer.

The present invention also provides a second method of forming a capacitor. First, an insulation layer pattern having a contact hole is formed on a substrate having a lower structure. Then, a first conductive layer is continuously on a sidewall portion and a bottom portion of the contact hole and on the surface of the insulation layer pattern. The first conductive layer formed on the surface portion of the insulation layer pattern is removed and the insulation layer pattern is removed to allow the first conductive layer to remain on the side wall portion and the bottom portion of the contact hole to form a cylindrical lower electrode. After that, a reaction-preventing layer is formed on the cylindrical lower electrode for preventing an oxidation at a temperature of not generating a

phase change of the lower electrode. A dielectric layer is formed on the reaction-preventing layer and a second conductive layer is formed on the dielectric layer as an upper electrode.

As described above, a reaction-preventing layer is formed at a low temperature of not generating a phase change of the lower electrode. Therefore, a thermal budget applied onto the lower electrode during forming the reaction-preventing layer can be remarkably reduced.

In addition, the method of the present invention can be positively applied for the formation of a capacitor having a high storage capacity by applying metal oxide having a high dielectric constant in forming a dielectric layer, which will be described hereinafter.

Hereinafter, the embodiments of the present invention will be described in detail with reference to attached drawings.

FIGS. 1a to 1d are cross-sectional views for explaining a method of forming a capacitor of a semiconductor device according to a preferred embodiment of the present invention.

Referring to FIG. 1a, a first conductive layer 12 is formed on a substrate 10. At this time, the first conductive layer 12 is used as a lower electrode of a semiconductor device. Accordingly, an amorphous silicon layer, a polycrystalline silicon layer, and the like can be exemplified as the first conductive layer 12. It is preferable that these layers are used alone. However, it does not no matter that two or more layers thereof also are deposited to form a multi-layered structure, that is, a composite layer.

Referring to FIG. 1b, a reaction-preventing layer 14 is formed on the

first conductive layer 12. The reaction-preventing layer 14 prevents the formation of an oxide layer at an interface between the first conductive layer 12 and a dielectric layer during a subsequent process of forming the dielectric layer. In addition, the reaction-preventing layer 14 also is formed to facilitate the reaction of the first conductive layer 12 and the dielectric layer. As an example of the reaction-preventing layer 14 used in the present invention, a nitride layer may be mentioned. When the reaction-preventing layer 14 is formed at a high temperature, the phase of the first conductive layer 12 may be changed and a problem concerning a resistance might be generated. Therefore, it is preferable that the reaction-preventing layer 14 is formed at a temperature condition of not generating a phase change of the first conductive layer 12 and not affecting a contact resistance.

When a nitride layer is formed on the first conductive layer 12 as the reaction-preventing layer 14, the processing condition is as follows.

When the first conductive layer 12 is an amorphous silicon layer and when the temperature during forming the nitride layer is up to about 700°C, the amorphous silicon is transformed into crystalline silicon. In conclusion, when the temperature exceeds about 600°C, the phase of the first conductive layer 12 changes. Therefore, it is that preferable that nitride layer is formed at a temperature of about 600°C or less.

When considering the above-described condition, the nitride layer is preferably formed by a plasma nitration method at a temperature of about 600°C or less, by a chemical vapor deposition method at a temperature of about 600°C or less or by an atomic layer deposition method at a temperature of

about 600°C or less.

A method of forming the nitride layer by the plasma nitration method having a temperature condition of about 600°C or less is as follows.

First, the temperature of the inner portion of a processing chamber is set to about 600°C. Then, NH_3 gas or N_2 gas is provided into the processing chamber and plasma is applied to the NH_3 gas or the N_2 gas. A nitration at the surface portion of the first conductive layer 12 is accomplished to form a nitride layer on the first conductive layer.

The nitride layer may be formed at the temperature of about 600°C or less because a kinetic energy is additionally applied as well as a thermal energy. According to the conventional rapid thermal nitration method, only the thermal energy is utilized and so the temperature should be set to about 700°C or over.

On the contrary, according to the plasma nitration method of the present invention, the temperature of up to about 600°C is sufficient. Therefore, the thermal energy owing to the temperature difference should be complemented when the plasma nitration method is implemented according to the present invention. According to the plasma nitration method, the kinetic energy by the plasma is additionally applied in addition to the thermal energy. That is, the thermal energy difference due to the temperature difference is obtained from the kinetic energy by the plasma.

A method of forming the nitride layer by the chemical vapor deposition method at the temperature of about 600°C or less is as follows.

First, the temperature of the inner portion of the processing chamber is set to about 550°C. Into the processing chamber, a gas including silicon and a

gas including nitrogen are provided as a gas source. The gas including silicon and the gas including nitrogen are excited utilizing plasma. Then, the gas including silicon and nitrogen are reacted with each other to form a nitride compound. Thus formed nitride compound is deposited on the first conductive layer 12. Through continuing the deposition, a nitride layer having an appropriate thickness is obtained. That is, the formation of the nitride layer as the reaction-preventing layer 14 by the chemical vapor deposition method is accomplished not through a nitration of the surface portion of the first conductive layer 12 but through a repeated deposition of the nitride compound.

As described above, because the nitride layer is formed through a chemical vapor deposition method, the temperature condition of about 600°C or less is applicable.

Hereinafter, a method of forming a nitride layer through an atomic layer deposition method at a temperature of about 600°C or less will be described.

First, the temperature of the inner portion of a processing chamber is set to about 550°C. Then, a first reacting material is introduced into the processing chamber. As the first reacting material, a source gas including silicon can be used. When introducing the first reacting material, a portion of the first reacting material is chemically absorbed (referred to as chemisorbed) on the first conductive layer 12.

After that, an inert gas is introduced into the processing chamber. Through the introduction of the inert gas, the first reacting material physically absorbed (referred to as physisorbed) on the first conductive layer 12 is removed. An example of the inert gas is argon. The removal of the first reacting

material is accomplished by purging utilizing the inert gas or by a vacuum pumping. The purging or the vacuum pumping can be independently applied. However, it is preferable that the purging and the vacuum pumping are subsequently applied. The physically absorbed first reacting material is removed from the first conductive layer 12 through the purging and/or vacuum pumping as described above.

A second reacting material is introduced into the processing chamber. A source gas including nitrogen is an example of the second reacting gas. Here, when the first reacting material is the source gas including silicon, the second reacting gas is the source gas including nitrogen. However, when the first reacting material is the source gas including nitrogen, the second reacting gas is the source gas including silicon. Through introducing the second reacting material, a portion of the second reacting material is chemically absorbed onto the first conductive layer 12.

Then, an inert gas is introduced into the processing chamber. Through introducing the inert gas, the second material physically absorbed onto the first conductive layer 12 is removed. An example of the inert gas is argon. At this time, the removal of the second reacting material is accomplished through a purging utilizing the inert gas or a vacuum pumping as for the first reacting material. The purging or the vacuum pumping can be independently applied, however, it is preferable that both the purging and the vacuum pumping are subsequently applied. As described above, the physically absorbed second reacting material is removed from the first conductive layer 12 through the purging and/or vacuum pumping.

At last, the first reacting material and the second reacting material are chemically absorbed onto the first conductive layer 12. That is, a solid material including the first reacting material and the second reacting material is formed on the first conductive layer 12. Through repeating the introduction of the first reacting material, the purging (and selectively vacuum pumping), the introduction of the second reacting material and the purging (and selectively vacuum pumping), a nitride layer as the reaction preventing layer 14 is formed on the first conductive layer 12. A nitride layer having a desired thickness can be obtained by controlling the number of repeating times of the above-described sub-processes.

In particular, when the nitride layer as the reaction preventing layer 14 is formed by the atomic layer deposition method, the nitride layer having a thickness of from several Å to several tens Å can be advantageously formed. Accordingly, it is preferable that the reaction-preventing layer 14 is formed through this atomic layer deposition method.

Besides the plasma nitration method, the chemical vapor deposition method and the atomic layer deposition method, a microwave-type deposition method can be used for the formation of the nitride layer. Since a kinetic energy also is additionally generated through the microwave-type deposition method, the temperature condition of about 600°C or less also can be applied.

Referring to FIG. 1c, a dielectric layer 16 is formed on the reaction-preventing layer 14. The dielectric layer 16 can be a metal oxide layer. That is, even though the dielectric layer 16 is formed under an oxygen atmosphere, the first conductive layer 12, i.e. a lower electrode is not reactive under the oxygen

atmosphere. The reaction-preventing layer 14 shields the reaction of the lower electrode with the oxygen atmosphere. The dielectric layer 16 can be a metal oxide layer including TiO_2 layer, Al_2O_3 layer, Y_2O_3 layer, ZrO_2 layer, HfO_2 layer, $BaTiO_3$ layer, $SrTiO_3$ layer, etc. It is preferable that one of these layers is used alone. However, two or more layers can be subsequently deposited to form a composite layer. At this time, the metal oxide layer formed as the dielectric layer excludes Ta_2O5 layer because a crystallization and heat treatment should be implemented at about 600°C or over after forming the Ta_2O_5 layer.

According to the present invention, a process for post-treating the dielectric layer 16 is not implemented after forming the metal oxide layer as the dielectric layer 16. In addition, it is preferable that the dielectric layer 16, that is, the metal oxide layer is formed by a chemical vapor deposition method at a temperature of about 600°C or less or by an atomic layer deposition method at a temperature of about 600°C or less.

A method of forming the dielectric layer 16 by the chemical vapor deposition method at a temperature of about 600°C or less is as follows.

First, the temperature of the inner portion of a processing chamber is set to about 600°C. Then, a source gas is provided into the processing chamber. The kind of the source gas is selected considering the kind of a thin film to be formed. For example, a gas including Al and a gas including O are provided into the processing chamber to form an Al_2O_3 layer.

Then, the gas source is excited using plasma. Accordingly, a reaction product of the gas sources is deposited on the reaction-preventing layer 14. Through continuing the deposition, a dielectric layer 16 having a predetermined

thickness is formed on the reaction-preventing layer 14.

A method of forming the dielectric layer 16 by the atomic layer deposition method at a temperature of about 600°C or less, is as follows.

First, the temperature of the inner portion of the processing chamber is set to about 600°C and more preferably to about 450°C. Then, a third reacting material is introduced into the processing chamber. The kind of the third material is selected according to the kind of the thin film to be formed. When forming a metal oxide layer, the preferred third reacting material includes a metal precursor. Through introducing the third material, a portion of the third material is chemically absorbed on the reaction-preventing layer 14.

Then, an inert gas is introduced into the processing chamber. Through introducing the inert gas, a physically absorbed third reacting material on the reaction-preventing layer 14 is removed. An example of the inert gas is argon. Here, the removal of the third reacting material is accomplished by a purging process utilizing the inert gas or by a vacuum pumping process. The purging and the vacuum pumping can be independently implemented. However, it is preferable that both the purging and the vacuum pumping can be subsequently implemented. The physically absorbed third reacting material is removed from the reaction-preventing layer 14 by the purging and/or vacuum pumping.

A fourth reacting material is introduced into the processing chamber. The fourth reacting material is an oxidizing agent. When introducing the fourth reacting material into the processing chamber, a portion of the second reacting material is chemically absorbed onto the reaction-preventing layer 14.

Thereafter, an inert gas is introduced into the processing chamber.

When introducing the inert gas, physically absorbed fourth reacting material onto the reaction-preventing layer 14 can be removed. An example of the inert gas is argon. At this time, the removal of the fourth reacting material is accomplished via a purging process utilizing the inert gas or a vacuum pumping as for the removal of the third reacting material. The purging or the vacuum pumping can be independently implemented, however, preferably, both the two methods are subsequently implemented. By the purging and/or vacuum pumping, the physically absorbed fourth material is removed from the reaction-preventing layer 14.

Accordingly, the third reacting material and the fourth reacting material are chemically absorbed onto the reaction-preventing layer 14. That is, a solid material including the third reacting material and the fourth reacting material is formed on the reaction-preventing layer 14. In addition, through repeating the processes of introducing the third reacting material, the purging (and selectively vacuum pumping), the introducing of the fourth material and purging (and selectively vacuum pumping), and the purging (and selectively vacuum pumping), the dielectric layer 16 is formed on the reaction preventing layer 14. Further, the dielectric layer 16 having a desired thickness can be obtained by controlling the number of repeating times.

Referring to FIG. 1d, a second conductive layer 18 as an upper electrode is formed on the dielectric layer 16. The second conductive layer 18 can be an amorphous silicon layer, a polycrystalline silicon layer, a Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer, and the like. Preferably, one of these layers is used alone. However, two or more layers can be

subsequently deposited to form a multi-layered composite layer.

After completing the above-described processes, a capacitor including the lower electrode, the dielectric layer and the upper electrode is formed on the substrate. The capacitor is designated by cap in FIG. 1d.

Here, the reaction-preventing layer is formed between the lower electrode and the dielectric layer. The dielectric layer can be a metal oxide layer having a high dielectric constant. In particular, all of the processes for forming the capacitor are implemented at a temperature of about 600°C or less. Since the process for forming the capacitor is carried out at such a low temperature, a thermal damage due to the processing temperature during forming the capacitor can be remarkably decreased. Therefore, the deterioration of the capacitor function induced by the thermal damage can be reduced to improve a reliability of the capacitor.

In the embodiment described above, the capacitor is shown as a simple plate type. However, all types of capacitors including a cylindrical shape, a pin shape, etc. can be applied in the present invention.

Hereinafter, a method of forming a cylindrical capacitor according to a preferred embodiment of the present invention will be described in detail.

FIGS. 2a to 2g are cross-sectional views of explaining a method of forming a cylindrical capacitor of a semiconductor device according to a preferred embodiment of the present invention.

Referring to FIG. 2a, a trench structure 202 is formed at an upper portion of a substrate 200 through implementing an isolation process. Accordingly, the substrate 200 is separated into an active region and a non-

active (field) region. A p-well and an n-well are formed by partially implanting impurities into the substrate 200. Then, gate patterns 204 including a polysilicon 204a, a tungsten silicide 204b and a silicon nitride 204c are formed on the active region of the substrate 200. The gate patterns 204 are provided as word lines of a DRAM device. The gate pattern 204 includes a polycide structure formed by stacking the impurity-doped polysilicon 204a and the tungsten silicide 204b. On the sidewall portion of the gate pattern 204, a spacer 206 of silicon nitride can be further formed.

Here, impurities are implanted into the upper portion of the substrate 200 neighboring the gate patterns 204 utilizing the gate patterns 204 as a mask to form a source 205a / a drain 205b. Accordingly, a transistor structure including the gate pattern 204, the source 205a / the drain 205b is obtained. Here, one of the source 205a and the drain 205b of the transistor structure is a capacitor contact region for connecting to a lower electrode of the capacitor and the other one is a bit line contact region for connecting to a bit line structure. According to a preferred embodiment of the present invention, the source 205a corresponds to the capacitor contact region and the drain 205b corresponds to the bit line contact region.

A capacitor contact pad 210a for electrically connecting the lower electrode of the capacitor to the source 205a and a bit line contact pad 210b for electrically connecting the bit line structure to the drain 205b are formed by filling polysilicon between gate patterns 204 of the transistor structure. Here, the polysilicon 210 filled in the capacitor contact region corresponds to the capacitor contact pad 210a and the polysilicon 210 filled at the bit line contact region

corresponds to the bit line contact pad 210b.

Referring to FIG. 2b, a bit line structure 220 electrically contacting the bit line contact pad 210b to the drain 205b is formed. Particularly, a first interlayer dielectric 222 is deposited on the gate pattern 204 of the transistor structure and on the polysilicon 210 filled between the gate patterns 204. Then, a bit line contact hole 223 for exposing the surface of the bit line contact pad 210b is formed by partially etching the first interlayer dielectric 222 through a photolithography process. Thereafter, tungsten 220a is continuously deposited on the bit line contact hole 223 and the first interlayer dielectric 222. As a result, the tungsten 220a is completely filled within the bit line contact hole 223. Silicon nitride 220b is deposited on the tungsten 220a. Then, the silicon nitride 220b and the tungsten 220a are partially etched to form a bit line structure 220 including the tungsten 220a and the silicon nitride 220b through a photolithography process.

After that, silicon nitride is deposited on the bit line structure 220 and the first interlayer dielectric 222. A spacer structure 224 is formed on the sidewall portion of the bit line structure 220 through etching the silicon nitride. At last, the tungsten 220a of the bit line structure 220 is covered with the silicon nitride 220b of the mask layer and is surrounded by the silicon nitride of the spacer structure 224.

A second interlayer dielectric 230 is subsequently deposited on the bit line structure 220, the spacer structure 224 and the first interlayer dielectric 222. The second interlayer dielectric 230 includes silicon nitride and is deposited through a high-density plasma deposition process.

Referring to FIG. 2c, the second interlayer dielectric 230 and the first interlayer dielectric 222 are continuously etched to form a self-aligned contact hole 232 for exposing the surface portion of the capacitor contact pad 210a. The etching is accomplished by using a difference of etching rates of the silicon nitride of the bit line structure 220 and the spacer structure 224 and the silicon oxide of the second interlayer dielectric 230 and the first interlayer dielectric 222.

Referring to FIG. 2d, a plug 234 for a lower electrode of the capacitor is filled within the self-aligned contact hole 232. The plug 234 for the lower electrode can be an amorphous silicon layer, a polycrystalline silicon layer, and the like. Preferably, one of these layers is formed alone, however, two or more layers can be deposited to form a composite layer.

Referring to FIG. 2e, a node for a lower electrode 234a connected to the plug 234 for a lower electrode and having a cylindrical shape is formed. At last, a lower electrode including the plug 234 and the node 234a is obtained. Here, the node 234a is preferably formed using the same material of the plug 234.

In particular, a method of forming the lower electrode including the plug 234 and the node 234a is as follows.

First, the plug 234 is filled within the self-aligned contact hole 232. Then, an oxide layer (not shown) is continuously formed on the second interlayer dielectric 230 and the plug 234. The oxide layer is patterned to have a cylindrical shape. Then, an electrode material for forming the node 234a is deposited on the patterned oxide layer having a cylindrical shape. The oxide layer is etched to form the lower electrode having a cylindrical shape.

Referring to FIG. 2f, a reaction-preventing layer 236 is formed on the surface portion of the lower electrode having the cylindrical shape. The reaction preventing layer 236 is formed to prevent the formation of an oxide layer at an interface of the lower electrode and the dielectric layer 237 during forming subsequent dielectric layer 237 and to prevent the generation of a contact resistance of a metal wiring. Here, an example of the reaction-preventing layer 236 is a nitride layer. When the reaction-preventing layer 236 is formed at a high temperature, the phase of the lower electrode may be changed and an adverse effect onto the contact resistance might be induced. Therefore, the reaction preventing layer 236 is preferably formed at a temperature of about 600°C or less so that the phase change of the lower electrode and the adverse effect onto the contact resistance are not induced.

After forming the reaction-preventing layer 236, a dielectric layer 237 is formed on the reaction-preventing layer 236. The dielectric layer 237 is formed via depositing the metal oxide described above. An example of the dielectric layer 237 is a TiO_2 layer, an Al_2O_3 layer, a Y_2O_3 layer, a ZrO_2 layer, a HfO_2 layer, a $BaTiO_3$ layer, a $SrTiO_3$ layer, and the like. One of these layers can be formed alone or two or more of these layers can be subsequently deposited to form the dielectric layer 237.

Here, after forming the metal oxide layer as the dielectric layer 237, a process of post-treatment of the dielectric layer 237 is not carried out. In particular, the dielectric layer 237, that is, the metal oxide layer is preferably formed by a chemical vapor deposition at a temperature of about 600°C or less or by an atomic layer deposition method at a temperature of about 600°C or

less.

Referring to FIG. 2g, a conductive material is deposited on the dielectric layer 237 as an upper electrode 238 of the capacitor. Then, the upper electrode 238 is formed on the dielectric layer 237. An example of the upper electrode 238 includes an amorphous silicon layer, a polycrystalline silicon layer, a Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer, etc.

At last, a capacitor of a semiconductor device including the lower electrode, the dielectric layer and the upper electrode is formed.

The process for forming the capacitor of the cylindrical shape is implemented at a temperature of about 600°C or less. Therefore, a thermal damage during forming the capacitor can be largely reduced. In addition, since the dielectric layer is formed as a metal oxide layer having a high dielectric constant, the storage capacity of the capacitor can be sufficiently increased. This result is obtainable thanks to the reaction-preventing layer to facilitate the formation of the dielectric layer.

The properties of the capacitor formed according to the method of the present invention will be described, hereinafter.

Preparation of sample 1

A polycrystalline silicon layer was formed as a lower electrode on a substrate. On the polycrystalline silicon layer, a nitride layer was formed as a reaction-preventing layer. The nitride layer was formed by an atomic layer deposition method at a temperature of about 550°C. After that, an Al_2O_3 layer was formed as a dielectric layer on the nitride layer. The Al_2O_3 layer was formed by the atomic layer deposition method at a temperature of about 450°C.

Thereafter, a composite layer of TiN layer and a polycrystalline silicon layer was formed on the Al2O3 layer as an upper electrode. After completing the above-described processes, sample 1 was obtained.

Preparation of sample 2

Sample 2 was prepared through implementing the same procedure described above for the preparation of sample 1, except that the nitride layer was formed by a rapid thermal nitration at a temperature of about 750°C and a heat treatment is implemented after forming the dielectric layer.

Measurements of contact resistance property

The contact resistances of sample 1 and sample 2 were measured. Thus obtained result is illustrated in FIG. 3.

FIG. 3 is a graph for explaining a contact resistance of a capacitor formed according to a preferred embodiment of the present invention. Referring to FIG. 3, the contact resistance of sample 1 is even further lower than that of sample 2.

Accordingly, a thermal damage is decreased when the capacitor is formed at a low temperature.

Twin bit defect

The twin bit defect means a contact between capacitor patterns through an inclination. When observing the twin bit defect of sample 1 and sample 2, the twin bit defect of sample 1 was found four per chip and the twin bit defect of

sample 2 was found about 20 per chip.

Accordingly, it can be noted that the thermal damage can be decreased when the reaction-preventing layer is formed at a low temperature.

[TECHNICAL EFFECT OF THE INVENTION]

As described above, the capacitor is formed at a low temperature of about 600°C or less. Therefore, a thermal damage onto the capacitor and the contact resistance can be largely decreased. In addition, a metal oxide layer having a high dielectric constant can be advantageously used as the dielectric layer. Accordingly, a semiconductor device having an improved reliability can be manufactured.

Although the preferred embodiments of the present invention have been described, it is understood that the present invention should not be limited to these preferred embodiments but various changes and modifications can be made by one skilled in the art within the spirit and scope of the present invention as hereinafter claimed.

[CLAIMS]

[CLAIM 1]

A method of forming a capacitor comprising:

forming a first conductive layer on a substrate;

forming a reaction-preventing layer on the first conductive layer to prevent an oxidation at a temperature of not generating a phase change of the first conductive layer;

forming a dielectric layer on the reaction preventing layer; and

forming a second conductive layer on the dielectric layer.

[CLAIM 2]

A method of forming a capacitor as claimed in claim 1, wherein the first conductive layer is an amorphous silicon layer, a polycrystalline silicon layer or a composite layer thereof.

[CLAIM 3]

A method of forming a capacitor as claimed in claim 1, wherein the reaction-preventing layer is a silicon nitride layer.

[CLAIM 4]

A method of forming a capacitor as claimed in claim 3, wherein the silicon nitride layer is formed by a plasma nitration method at a temperature of about 600°C or less.

[CLAIM 5]

A method of forming a capacitor as claimed in claim 3, wherein the silicon nitride layer is formed by a chemical vapor deposition method at a temperature of about 600°C or less or an atomic layer deposition method at a

temperature of about 600°C or less.

[CLAIM 6]

A method of forming a capacitor as claimed in claim 3, wherein the silicon nitride layer is formed by a microwave-type deposition method at a temperature of about 600°C or less.

[CLAIM 7]

A method of forming a capacitor as claimed in claim 1, wherein the dielectric layer is a metal oxide layer.

[CLAIM 8]

A method of forming a capacitor as claimed in claim 7, wherein the metal oxide layer is at least one selected from the group consisting of a TiO_2 layer, an Al_2O_3 layer, an Y_2O_3 layer, a ZrO_2 layer, a HfO_2 layer, a $BaTiO_3$ layer, a $SrTiO_3$ layer and a composite layer thereof.

[CLAIM 9]

A method of forming a capacitor as claimed in claim 7, wherein the metal oxide layer is formed by a chemical vapor deposition method at a temperature of about 600°C or less or by an atomic layer deposition method at a temperature of about 600°C or less.

[CLAIM 10]

A method of forming a capacitor as claimed in claim 1, wherein the second conductive layer is an amorphous silicon layer, a polycrystalline silicon layer, a Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and a composite layer thereof.

[CLAIM 11]

A method of forming a capacitor comprising:

forming an insulation layer pattern having a contact hole on a substrate having a lower structure;

forming a first conductive layer continuously on a sidewall portion and a bottom portion of the contact hole and on the surface of the insulation layer pattern;

removing the first conductive layer formed on the surface portion of the insulation layer pattern;

removing the insulation layer pattern to allow the first conductive layer to remain on the sidewall portion and the bottom portion of the contact hole to form a cylindrical lower electrode;

forming a reaction-preventing layer on the cylindrical lower electrode for preventing an oxidation at a temperature of not generating a phase change of the lower electrode;

forming a dielectric layer on the reaction preventing layer; and

forming a second conductive layer on the dielectric layer as an upper electrode.

[CLAIM 12]

A method of forming a capacitor as claimed in claim 11, wherein the first conductive layer is an amorphous silicon layer, a polycrystalline silicon layer or a composite layer thereof.

[CLAIM 13]

A method of forming a capacitor as claimed in claim 11, wherein the reaction preventing layer is formed by a plasma nitration method at a

temperature of about 600°C or less, a chemical vapor deposition method at a temperature of about 600°C or less or an atomic layer deposition method at a temperature of about 600°C or less.

[CLAIM 14]

A method of forming a capacitor as claimed in claim 11, wherein the dielectric layer is at least one selected from the group consisting of a TiO_2 layer, an Al_2O_3 layer, a Y_2O_3 layer, a ZrO_2 layer, a HfO_2 layer, a $BaTiO_3$ layer, a $SrTiO_3$ layer and a composite layer thereof.

[CLAIM 15]

A method of forming a capacitor as claimed in claim 11, wherein the dielectric layer is formed by a chemical vapor deposition method at a temperature of about 600°C or less or by an atomic layer deposition method at a temperature of about 600°C or less.

[CLAIM 16]

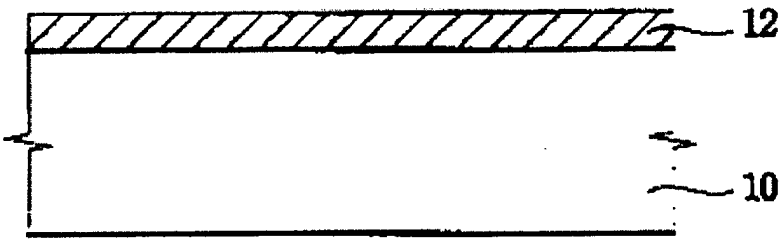
A method of forming a capacitor as claimed in claim 11, wherein the second conductive layer is one of an amorphous silicon layer, a polycrystalline silicon layer, a Ru layer, a Pt layer, an Ir layer, a TiN layer, a TaN layer, a WN layer and a composite layer thereof.

[CLAIM 17]

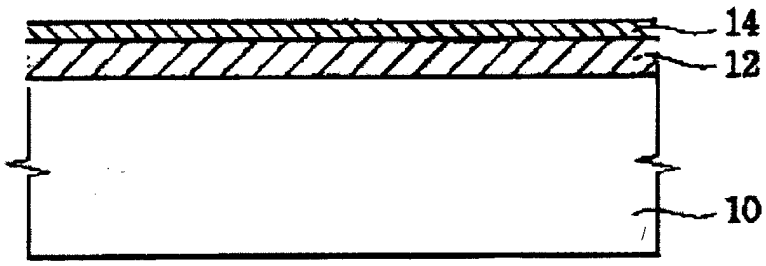
A method of forming a capacitor as claimed in claim 11, wherein the lower structure includes a contact plug connected to the lower electrode.

[DRAWINGS]

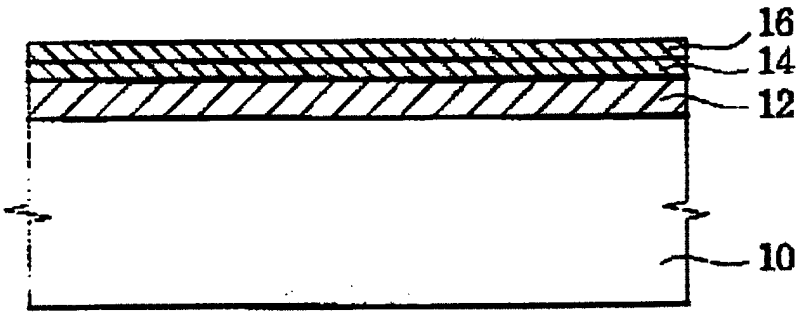
【FIG. 1a】



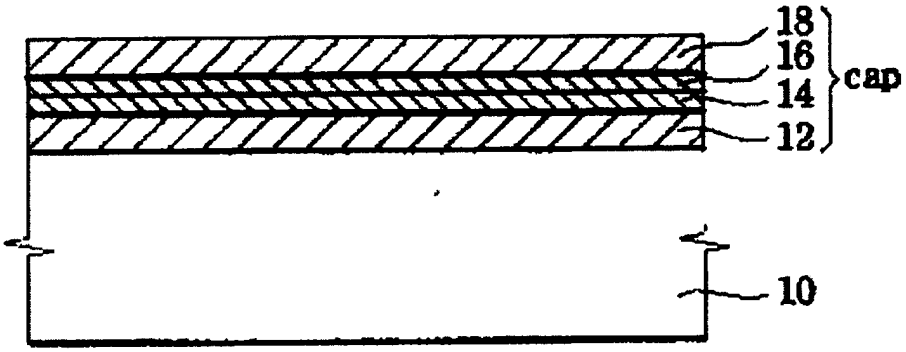
【FIG. 1b】



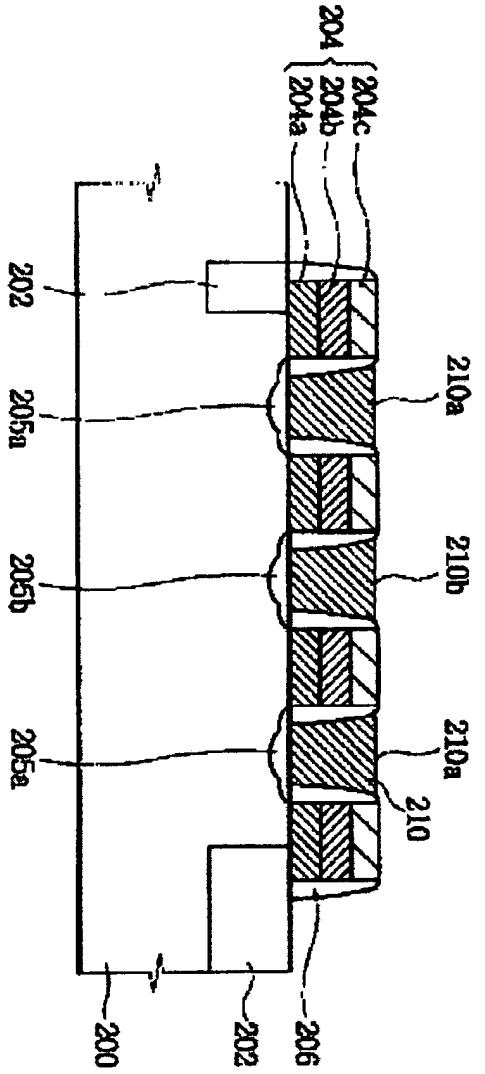
【FIG. 1c】



【FIG. 1d】



【FIG. 2a】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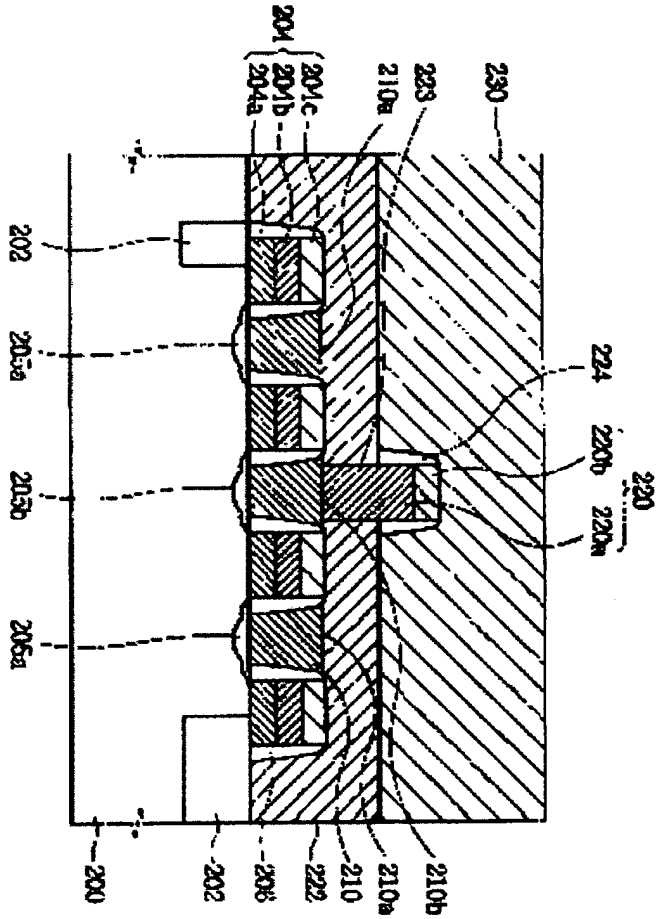
206

【FIG. 2b】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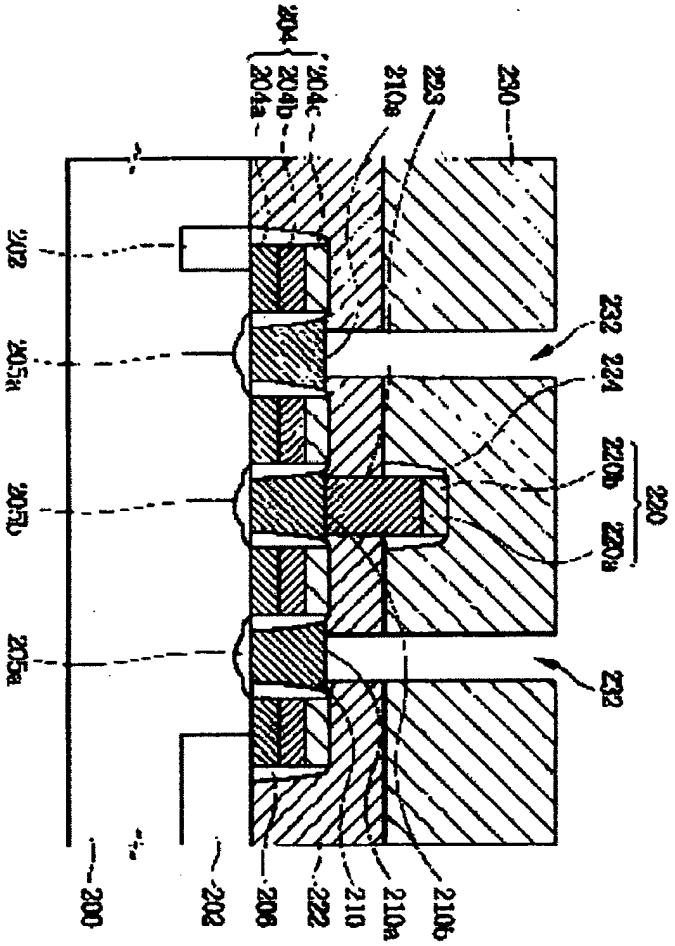
【FIG. 2c】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222
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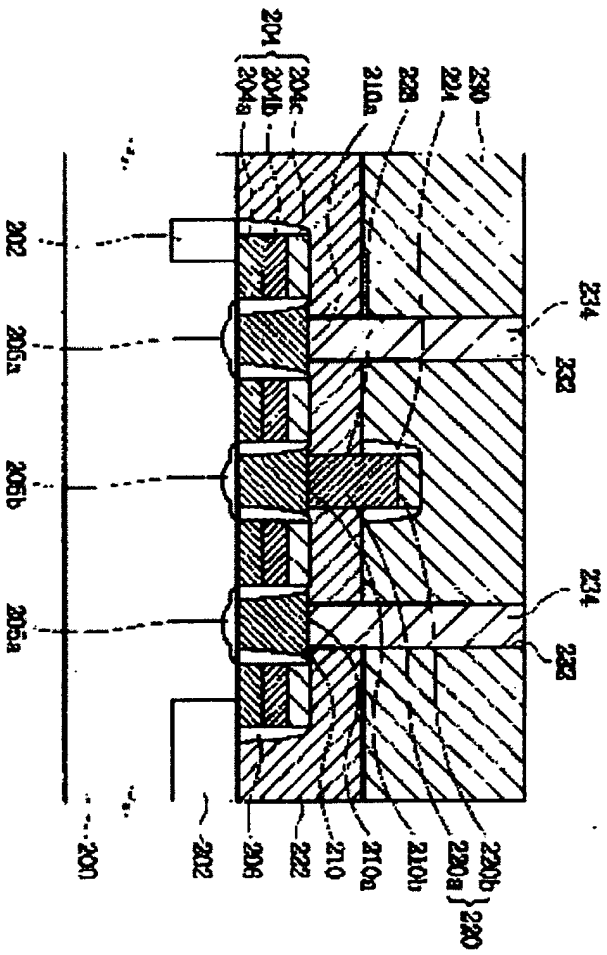
210b

【FIG. 2d】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210b
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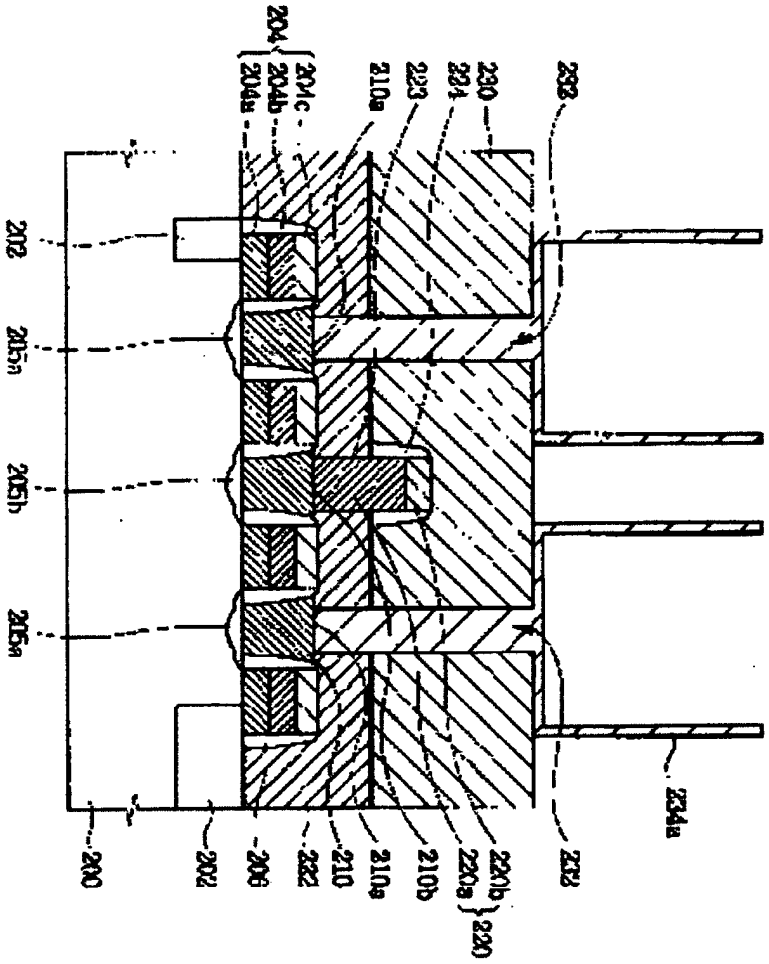
220b
220

【FIG. 2e】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232
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210b
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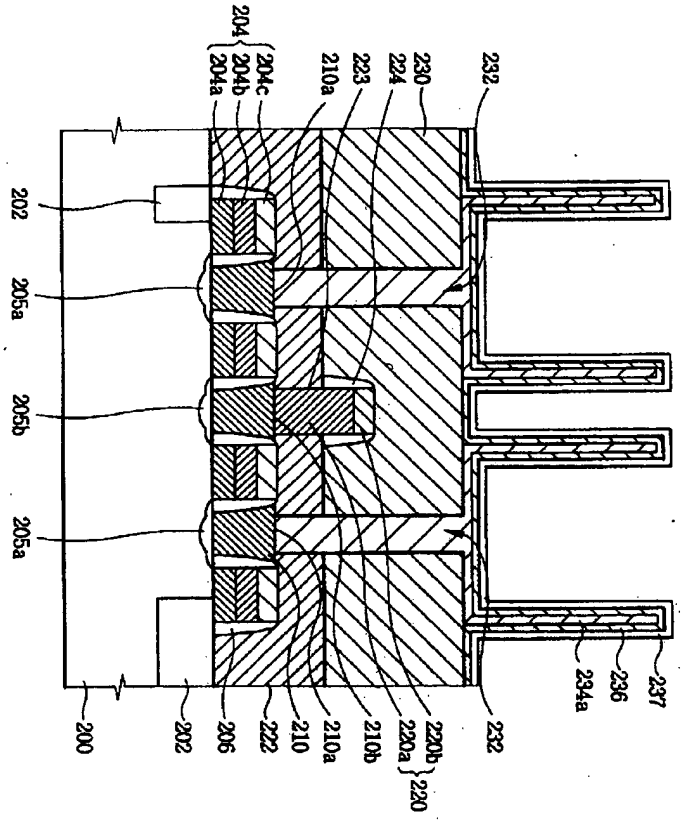
220b
220

【FIG. 2f】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205a
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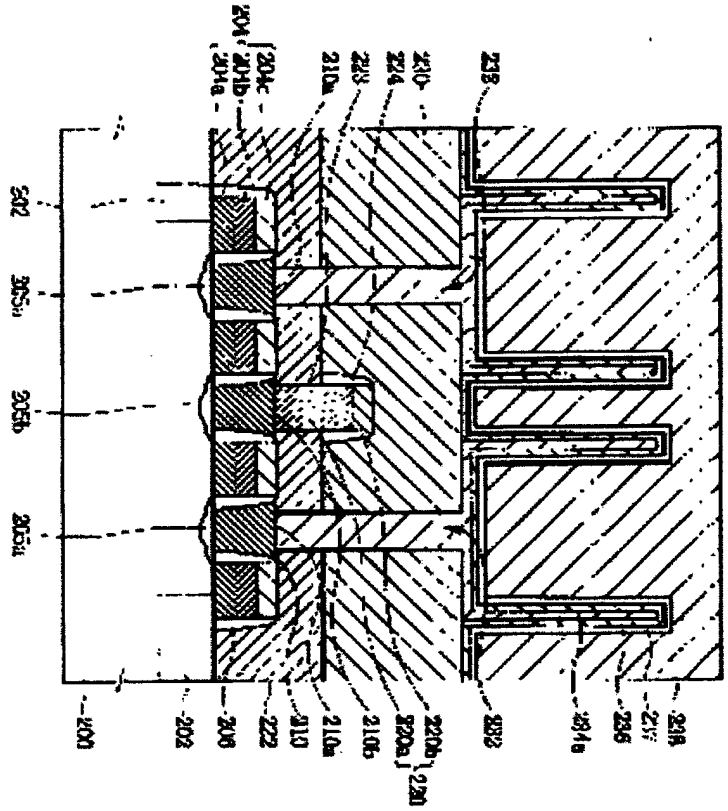
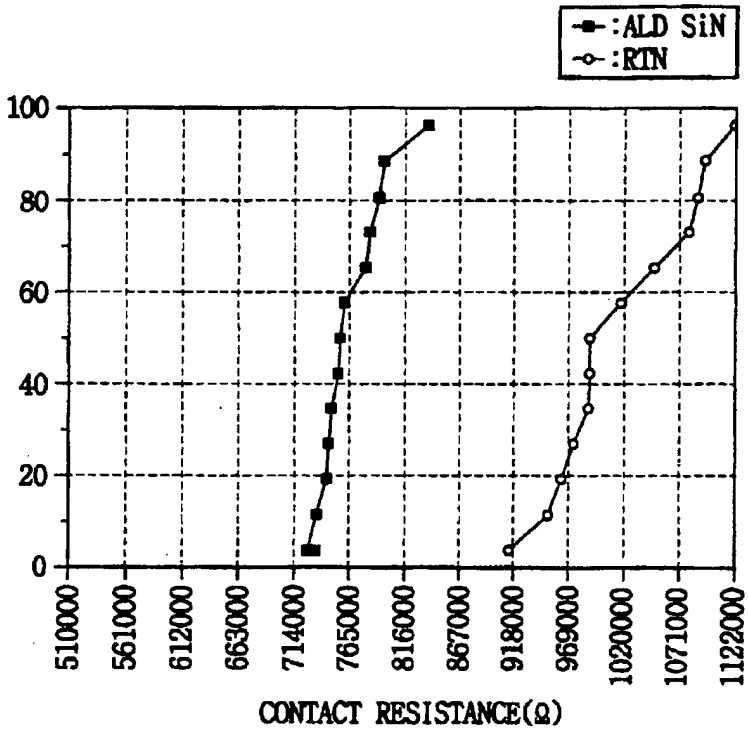
210b
220a
220b
220

【FIG. 2g】



【FIG. 3】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CONTACT RESISTANCE(Ω)